Dual Channel, 12-Bit, 80 MSPS A/D Converter with Analog Input Signal Conditioning

AD13280

FEATURES

Dual, 80 MSPS Minimum Sample Rate
- **Channel-to-Channel Matching, ±1% Gain Error**
- **90 dB Channel-to-Channel Isolation**
- **DC-Coupled Signal Conditioning**

80 dB Spurious-Free Dynamic Range
Selectable Bipolar Inputs (±1 V and ±0.5 V Ranges)
Integral Single-Pole Low Pass Nyquist Filter
Two's Complement Output Format
3.3 V Compatible Outputs
1.85 W per Channel
Industrial and Military Grade

APPLICATIONS

Radar Processing (Optimized for I/Q Baseband Operation)
Phased Array Receivers
Multichannel, Multimode Receivers
GPS Antijamming Receivers
Communications Receivers

PRODUCT DESCRIPTION

The AD13280 is a complete dual channel signal processing solution, including on-board amplifiers, references, ADCs, and output termination components to provide optimized system performance. The AD13280 has on-chip track-and-hold circuitry and utilizes an innovative multipass architecture to achieve 12-bit, 80 MSPS performance. The AD13280 uses innovative high density circuit design and laser-trimmed thin-film resistor networks to achieve exceptional channel matching, impedance control, and performance while still maintaining excellent isolation, and providing for significant board area savings.

Multiple options are provided for driving the analog input, including single-ended, differential, and optional series filtering. The AD13280 also offers the user a choice of analog input signal ranges to further minimize additional external signal conditioning, while still remaining general-purpose.

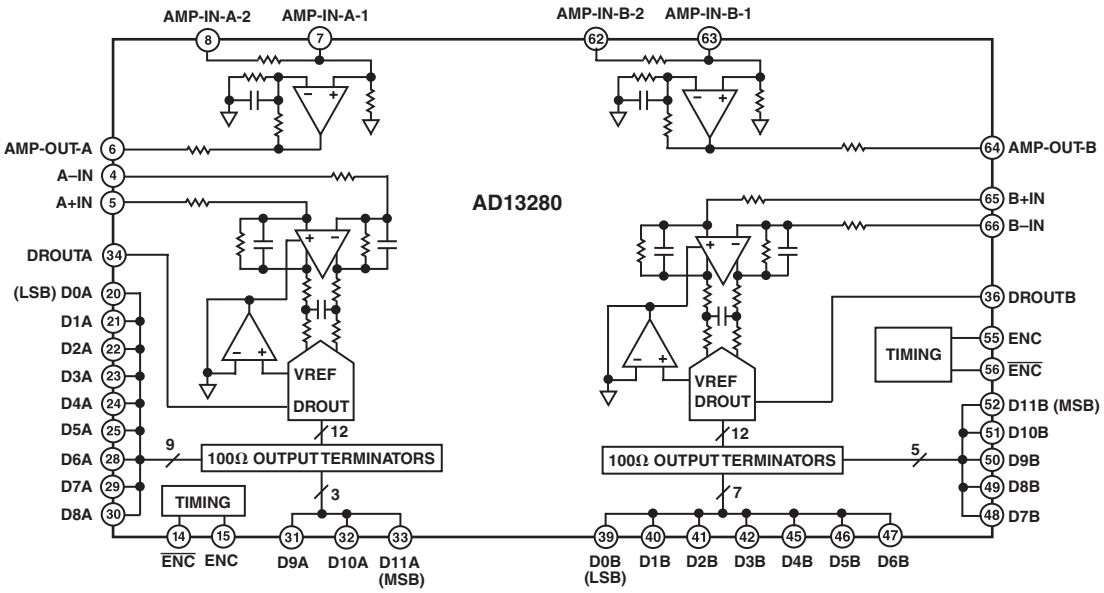
The AD13280 operates with ±5.0 V for the analog signal conditioning with a separate 5.0 V supply for the analog-to-digital conversion, and 3.3 V digital supply for the output stage. Each channel is completely independent, allowing operation with independent encode and analog inputs, and maintaining minimal crosstalk and interference.

The AD13280 is packaged in a 68-lead ceramic gull wing package. Manufacturing is done on Analog Devices' MIL-38534 Qualified Manufacturers Line (QML), and components are available up to Class-H (–40°C to +85°C). The components are manufactured using Analog Devices' high speed complementary bipolar process (XFCB).

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 80 MSPS.
2. Input signal conditioning included; gain and impedance match.
3. Single-ended, differential, or off-module filter options.
4. Fully tested/characterized full channel performance.
5. Compatible with 14-bit (up to) 65 MSPS family.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD13280–SPECIFICATIONS

(AV_{CC} = +5 V, AV_{EE} = –5 V, DV_{CC} = +3.3 V; applies to each ADC with Front-End Amplifier, unless otherwise noted.)

Parameter	Temp	Test Level	Mil Subgroup	AD13280AZ/BZ Min	Typ	Max	Unit
RESOLUTION					12		Bits
DC ACCURACY[1]							
No Missing Codes	Full	IV	12	Guaranteed			
Offset Error	25°C	I	1	–2.2	±1.0	+2.2	% FS
	Full	VI	2, 3	–2.2	±1.0	+2.2	% FS
Offset Error Channel Match	Full	VI	1, 2, 3	–1.0	±0.1	+1.0	%
Gain Error[2]	25°C	I	1	–3	–1.0	+1	% FS
	Full	VI	2, 3	–5.0	±2.0	+5.0	% FS
Gain Error Channel Match	25°C	I	1	–1.5	±0.5	+1.5	%
	Max	VI	2	–3.0	±1.0	+3.0	%
	Min	VI	3	–5	±1.0	+5	%
SINGLE-ENDED ANALOG INPUT							
Input Voltage Range							
AMP-IN-X-1	Full	V			±0.5		V
AMP-IN-X-2	Full	V			±1.0		V
Input Resistance							
AMP-IN-X-1	Full	IV	12	99	100	101	Ω
AMP-IN-X-2	Full	IV	12	198	200	202	Ω
Capacitance	25°C	V			4.0	7.0	pF
Analog Input Bandwidth[3]	Full	V			100		MHz
DIFFERENTIAL ANALOG INPUT							
Analog Signal Input Range							
A+IN to A–IN and B+IN to B–IN[4]	Full	V			±1		V
Input Impedance	25°C	V			618		Ω
Analog Input Bandwidth	Full	V			50		MHz
ENCODE INPUT (ENC, ENC)[1]							
Differential Input Voltage	Full	IV	12	0.4			V p-p
Differential Input Resistance	25°C	V			10		kΩ
Differential Input Capacitance	25°C	V			2.5		pF
SWITCHING PERFORMANCE							
Maximum Conversion Rate[5]	Full	VI	4, 5, 6	80			MSPS
Minimum Conversion Rate[5]	Full	IV	12			20	MSPS
Aperture Delay (t_A)	25°C	V			1.5		ns
Aperture Delay Matching	25°C	IV	12		250	500	ps
Aperture Uncertainty (Jitter)	25°C	V			0.3		ps rms
ENCODE Pulsewidth High at Max Conversion Rate	25°C	IV	12	4.75	6.25	8	ns
ENCODE Pulsewidth Low at Max Conversion Rate	25°C	IV	12	4.75	6.25	8	ns
Output Delay (t_{OD})	Full	V			5		ns
Encode, Rising to Data Ready, Rising Delay	Full	V			8.5		ns
SNR[1, 6]							
Analog Input @ 10 MHz	25°C	I	4	66.5	70		dBFS
	Min	II	6	64.5			dBFS
	Max	II	5	66.3			dBFS
Analog Input @ 21 MHz	25°C	I	4	66.5	70		dBFS
	Min	II	6	64			dBFS
	Max	II	5	66.3			dBFS
Analog Input @ 37 MHz	25°C	I	4	63	65		dBFS
	Min	II	6	61.5			dBFS
	Max	II	5	63			dBFS
SINAD[1, 7]							
Analog Input @ 10 MHz	25°C	I	4	66	69		dBFS
	Min	II	6	63.5			dBFS
	Max	II	5	66			dBFS
Analog Input @ 21 MHz	25°C	I	4	64	68.5		dBFS
	Min	II	6	63			dBFS
	Max	II	5	64			dBFS
Analog Input @ 37 MHz	25°C	I	4	54	59		dBFS
	Min	II	6	53			dBFS
	Max	II	5	54			dBFS

Parameter	Temp	Test Level	Mil Subgroup	AD13280AZ/BZ Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE[1, 8]							
Analog Input @ 10 MHz	25°C	I	4	75	80		dBFS
	Min	II	6	70			
	Max	II	5	75			
Analog Input @ 21 MHz	25°C	I	4	68	75		dBFS
	Min	II	6	67			
	Max	II	5	67			
Analog Input @ 37 MHz	25°C	I	4	56	62		dBFS
	Min	II	6	55			
	Max	II	5	55			
SINGLE-ENDED ANALOG INPUT							
Pass-Band Ripple to 10 MHz	25°C	V			0.05		dB
Pass-Band Ripple to 25 MHz	25°C	V			0.1		dB
DIFFERENTIAL ANALOG INPUT							
Pass-Band Ripple to 10 MHz	25°C	V			0.3		dB
Pass-Band Ripple to 25 MHz	25°C	V			0.82		dB
TWO-TONE IMD REJECTION[9]							
f_{IN} = 9.1 MHz and 10.1 MHz	25°C	I	4	75	80		dBc
f_1 and f_2 are –7 dB	Min	II	6	71			
	Max	II	5	74			
f_{IN} = 19.1 MHz and 20.7 MHz	25°C	V	4		77		dBc
f_1 and f_2 are –7 dB							
f_{IN} = 36 MHz and 37 MHz	25°C	V	4		60		dBc
f_1 and f_2 are –7 dB							
CHANNEL-TO-CHANNEL ISOLATION[10]	25°C	IV	12	90			dB
TRANSIENT RESPONSE	25°C	V			25		ns
DIGITAL OUTPUTS[11]							
Logic Compatibility					CMOS		
DVCC = 3.3 V							
Logic "1" Voltage	Full	I	1, 2, 3	2.5	DVCC – 0.2		V
Logic "0" Voltage	Full	I	1, 2, 3		0.2	0.5	V
DVCC = 5 V							
Logic "1" Voltage	Full	V			DVCC – 0.3		V
Logic "0" Voltage	Full	V			0.35		V
Output Coding					Two's Complement		
POWER SUPPLY							
AV_{CC} Supply Voltage[12]	Full	IV		4.85	5.0	5.25	V
I (AV_{CC}) Current	Full	I	1, 2, 3		310	338	mA
AV_{EE} Supply Voltage[12]	Full	IV		–5.25	–5.0	–4.75	V
I (AV_{EE}) Current	Full	I	1, 2, 3		38	49	mA
DV_{CC} Supply Voltage[12]	Full	IV		3.135	3.3	3.465	V
I (DV_{CC}) Current	Full	I	1, 2, 3		34	46	mA
I_{CC} (Total) Supply Current per Channel	Full	I	1, 2, 3		369	433	mA
Power Dissipation (Total)	Full	I	1, 2, 3		3.72	4.05	W
Power Supply Rejection Ratio (PSRR)	Full	V			0.01		% FSR/% V_S

NOTES

[1] All ac specifications tested by driving ENCODE and ENCODE differentially. Single-ended input: AMP-IN-X-1 = 1 V p-p, AMP-IN-X-2 = GND.

[2] Gain tests are performed on AMP-IN-X-1 input voltage range.

[3] Full Power Bandwidth is the frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

[4] For differential input: +IN = 1 V p-p and –IN = 1 V p-p (signals are 180° out of phase). For single-ended input: +IN = 2 V p-p and = –IN = GND.

[5] Minimum and maximum conversion rates allow for variation in Encode Duty Cycle of 50% ± 5%.

[6] Analog Input signal power at –1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed). Encode = 80 MSPS. SNR is reported in dBFS, related back to converter full scale.

[7] Analog Input signal power at –1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. Encode = 80 MSPS. SINAD is reported in dBFS, related back to converter full scale.

[8] Analog Input signal at –1 dBFS; SFDR is the ratio of converter full scale to worst spur.

[9] Both input tones at –7 dBFS; two-tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third order intermod product.

[10] Channel-to-channel isolation tested with A channel grounded and a full-scale signal applied to B Channel.

[11] Digital output logic levels: DV_{CC} = 3.3 V, C_{LOAD} = 10 pF. Capacitive loads >10 pF will degrade performance.

[12] Supply voltage recommended operating range. AV_{CC} may be varied from 4.85 V to 5.25 V. However, rated ac (harmonics) performance is valid only over the range AV_{CC} = 5.0 V to 5.25 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL[1]

AV_{CC} Voltage	0 V to 7 V
AV_{EE} Voltage	–7 V to 0 V
DV_{CC} Voltage	0 V to 7 V
Analog Input Voltage	V_{EE} to V_{CC}
Analog Input Current	–10 mA to +10 mA
Digital Input Voltage (ENCODE)	0 to V_{CC}
ENCODE, $\overline{\text{ENCODE}}$ Differential Voltage	4 V max
Digital Output Current	–10 mA to +10 mA

ENVIRONMENTAL[2]

Operating Temperature (Case)	–40°C to +85°C
Maximum Junction Temperature	175°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	–65°C to +150°C

NOTES

[1]Absolute maximum ratings are limiting values applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedance for "ES" package: θ_{JC} 2.2°C/W; θ_{JA} 24.3°C/W.

TEST LEVEL

I. 100% Production Tested

II. 100% Production Tested at 25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III. Sample Tested Only

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested with temperature at 25°C; sample tested at temperature extremes.

ORDERING GUIDE

Model	Temperature Range (Case)	Package Description	Package Option
AD13280AZ	–25°C to +85°C	68-Lead Ceramic Leaded Chip Carrier	ES-68C
AD13280AF	–25°C to +85°C	68-Lead Ceramic Leaded Chip Carrier with Nonconductive Tie-Bar	ES-68C
5962-0053001HXA	–40°C to +85°C	68-Lead Ceramic Leaded Chip Carrier	ES-68C
AD13280/PCB	25°C	Evaluation Board with AD13280AZ	

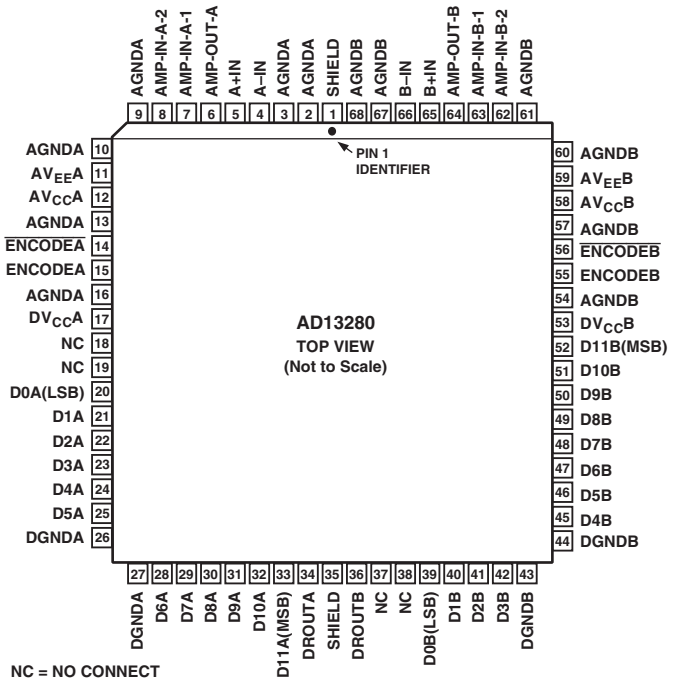
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD13280 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

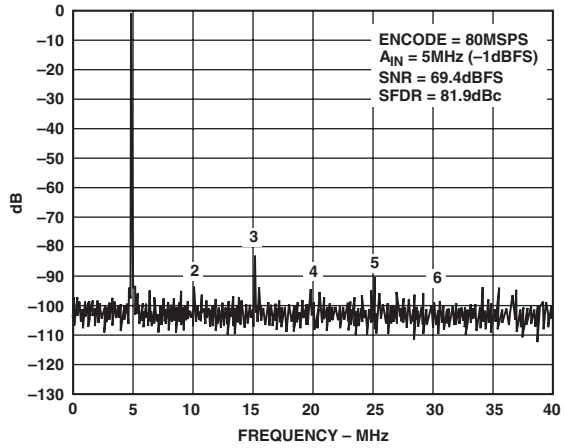
PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
1, 35	SHIELD	Internal Ground Shield between Channels
2, 3, 9, 10, 13, 16	AGNDA	A Channel Analog Ground. A and B grounds should be connected as close to the device as possible.
4	A–IN	Inverting Differential Input (Gain = 1)
5	A+IN	Noninverting Differential Input (Gain = 1)
6	AMP-OUT-A	Single-Ended Amplifier Output (Gain = 2)
7	AMP-IN-A-1	Analog Input for A Side ADC (Nominally ±0.5 V)
8	AMP-IN-A-2	Analog Input for A Side ADC (Nominally ±1.0 V)
11	$AV_{EE}A$	A Channel Analog Negative Supply Voltage (Nominally –5.0 V or –5.2 V)
12	$AV_{CC}A$	A Channel Analog Positive Supply Voltage (Nominally 5.0 V)
14	$\overline{\text{ENCODEA}}$	Complement of Encode; Differential Input
15	ENCODEA	Encode Input; Conversion Initiated on Rising Edge
17	$DV_{CC}A$	A Channel Digital Positive Supply Voltage (Nominally 5.0 V/ 3.3 V)
18, 19, 37, 38	NC	No Connect
20–25, 28–33	D0A–D11A	Digital Outputs for ADC A. D0 (LSB)
26, 27	DGNDA	A Channel Digital Ground
34	DROUTA	Data Ready A Output
36	DROUTB	Data Ready B Output
39–42, 45–52	D0B–D11B	Digital Outputs for ADC B. D0 (LSB)
43, 44	DGNDB	B Channel Digital Ground
53	$DV_{CC}B$	B Channel Digital Positive Supply Voltage (Nominally 5.0 V/ 3.3 V)
54, 57, 60, 61, 67, 68	AGNDB	B Channel Analog Ground. A and B grounds should be connected as close to the device as possible.
55	ENCODEB	Encode Input. Conversion initiated on rising edge.
56	$\overline{\text{ENCODEB}}$	Complement of Encode. Differential input.
58	$AV_{CC}B$	B Channel Analog Positive Supply Voltage (Nominally 5.0 V)
59	$AV_{EE}B$	B Channel Analog Negative Supply Voltage (Nominally –5.0 V or –5.2 V)
62	AMP-IN-B-2	Analog Input for B Side ADC (Nominally ±1.0 V)
63	AMP-IN-B-1	Analog Input for B Side ADC (Nominally ±0.5 V)
64	AMP-OUT-B	Single-Ended Amplifier Output (Gain = 2)
65	B+IN	Noninverting Differential Input (Gain = 1)
66	B–IN	Inverting Differential Input (Gain = 1)

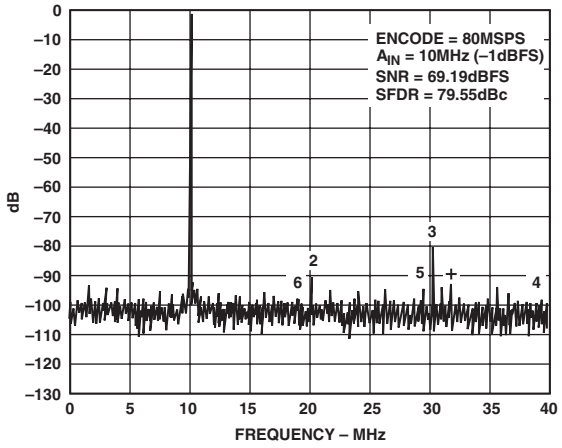
PIN CONFIGURATION



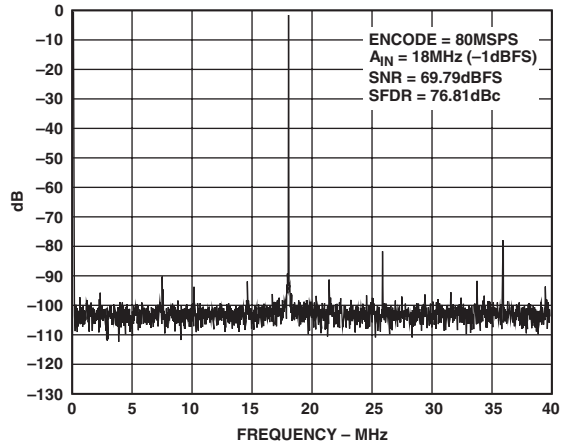
AD13280–Typical Performance Characteristics



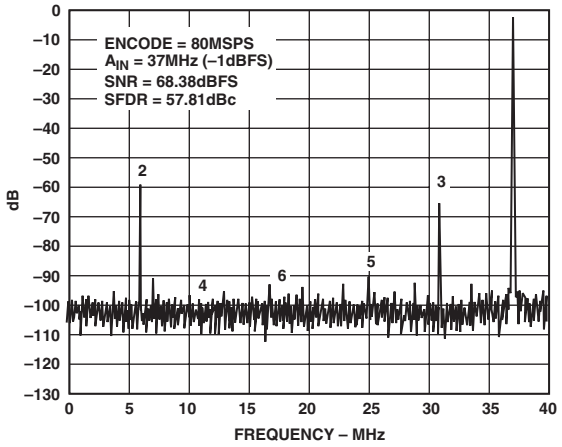
TPC 1. Single Tone @ 5 MHz



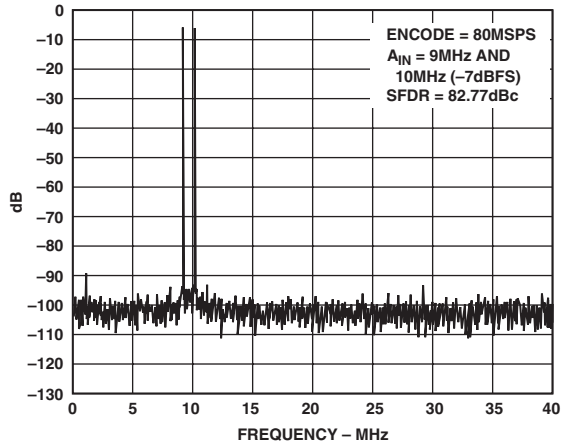
TPC 4. Single Tone @ 10 MHz



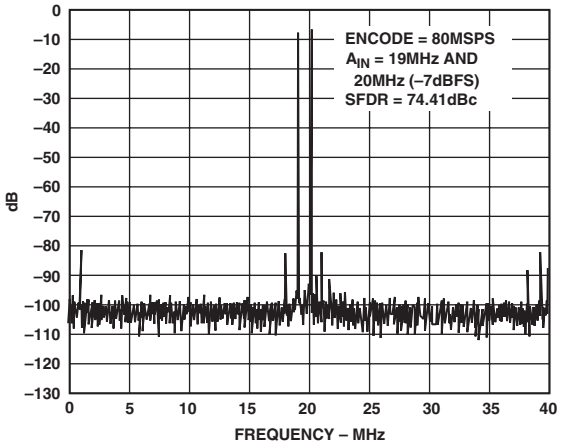
TPC 2. Single Tone @ 18 MHz



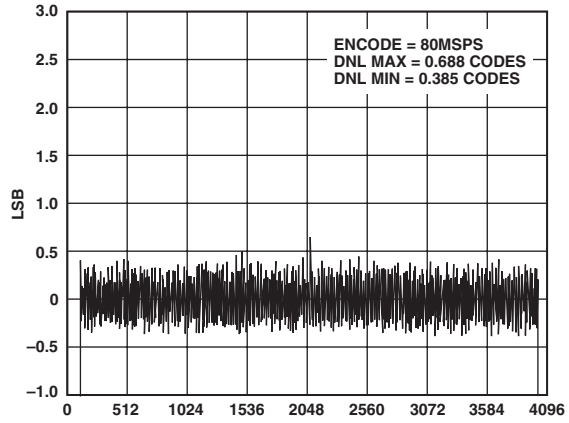
TPC 5. Single Tone @ 37 MHz



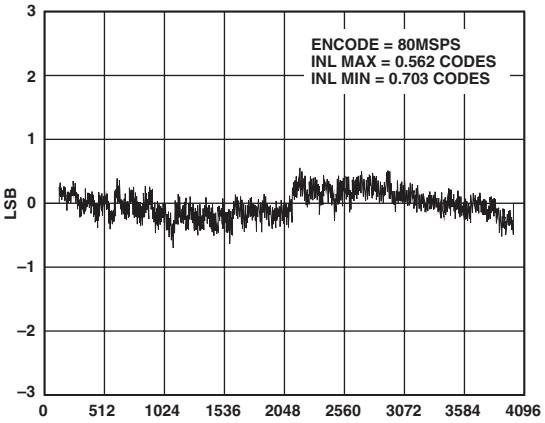
TPC 3. Two Tone @ 9 MHz/10 MHz



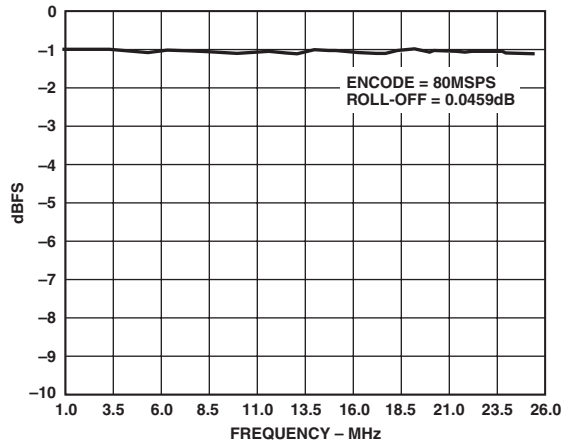
TPC 6. Two Tone @ 19 MHz/20 MHz



TPC 7. Differential Nonlinearity



TPC 9. Integral Nonlinearity



TPC 8. Pass-Band Ripple to 25 MHz

DEFINITION OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of the ENCODE and $\overline{\text{ENCODE}}$ command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic "1" state to achieve rated performance; pulsewidth low is the minimum time the ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable encode duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of the ENCODE and $\overline{\text{ENCODE}}$ command and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 0.02% accuracy after an analog input signal of the specified percentage of full scale is reduced to midscale.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc. May be reported in dB (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc. May be reported in dB (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Spurious-Free Dynamic Range
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic.

Transient Response
The time required for the converter to achieve 0.02% accuracy when a one-half full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

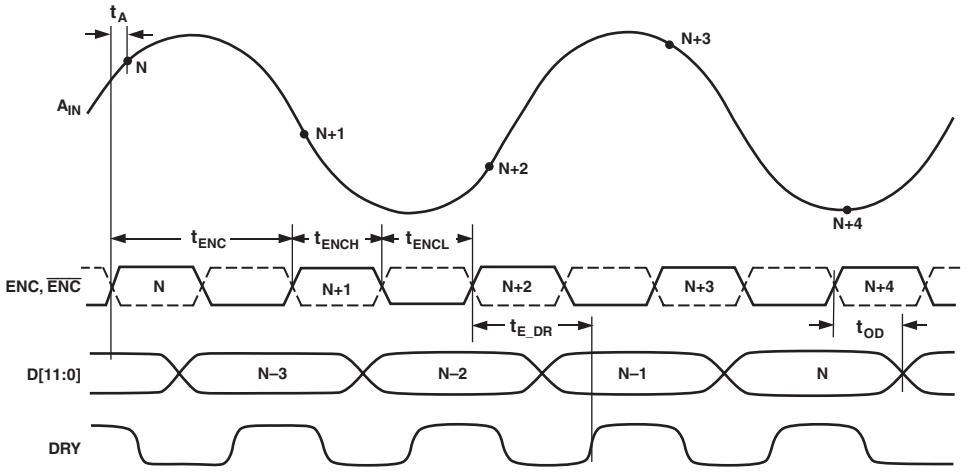


Figure 1. Timing Diagram

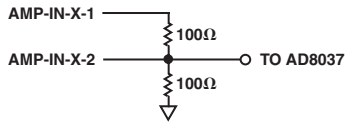


Figure 2. Single-Ended Input Stage

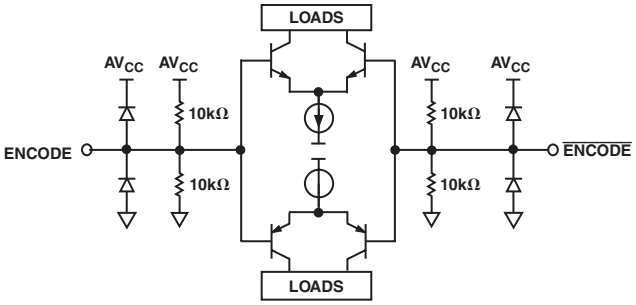


Figure 3. ENCODE Inputs

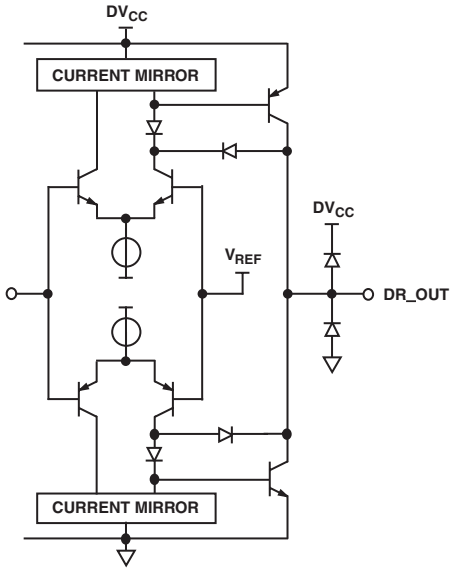


Figure 4. Digital Output Stage

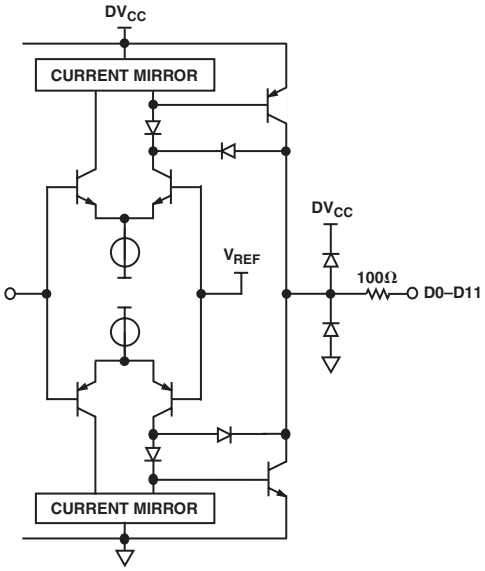


Figure 5. Digital Output Stage

THEORY OF OPERATION

The AD13280 is a high dynamic range 12-bit, 80 MHz pipeline delay (three pipelines) analog-to-digital converter. The custom analog input section provides input ranges of 1 V and 2 V p-p and input impedance configurations of 50 Ω, 100 Ω, and 200 Ω.

The AD13280 employs four monolithic ADI components per channel (AD8037, AD8138, AD8031, and a custom ADC IC), along with multiple passive resistor networks and decoupling capacitors to fully integrate a complete 12-bit analog-to-digital converter.

In the single-ended input configuration, the input signal is passed through a precision laser-trimmed resistor divider allowing the user to externally select operation with a full-scale signal of ±0.5 V or ±1.0 V by choosing the proper input terminal for the application. The result of the resistor divider is to apply a full-scale input approximately 0.4 V to the noninverting input of the internal AD8037 amplifier.

The AD13280 analog input includes an AD8037 amplifier featuring an innovative architecture that maximizes the dynamic range capability on the amplifier's inputs and outputs. The AD8037 amplifier provides a high input impedance and gain for driving the AD8138 in a single-ended to differential amplifier configuration. The AD8138 has a –3 dB bandwidth at 300 MHz and delivers a differential signal with the lowest harmonic distortion available in a differential amplifier. The AD8138 differential outputs help balance the differential inputs to the custom ADC, maximizing the performance of the device.

The AD8031 provides the buffer for the internal reference analog-to-digital converter. The internal reference voltage of the custom ADC is designed to track the offsets and drifts and is used to ensure matching over an extended temperature range of operation. The reference voltage is connected to the output common-mode input on the AD8138. This reference voltage sets the output common mode on the AD8138 at 2.4 V, which is the midsupply level for the ADC.

The custom ADC has complementary analog input pins, $\overline{\text{AIN}}$ and AIN. Each analog input is centered at 2.4 V and should swing ±0.55 V around this reference. Since AIN and $\overline{\text{AIN}}$ are 180 degrees out of phase, the differential analog input signal is 2.2 V peak-to-peak. Both analog inputs are buffered prior to the first track-and-hold.

The custom ADC digital outputs drive 100 Ω series resistors (Figure 5). The result is a 12-bit parallel digital CMOS-compatible word, coded as two's complement.

USING THE SINGLE-ENDED INPUT

The AD13280 has been designed with the user's ease of operation in mind. Multiple input configurations have been included on-board to allow the user a choice of input signal levels and input impedance. The standard inputs are ±0.5 V and 1.0 V. The user can select the input impedance of the AD13280 on any input by using the other inputs as alternate locations for the GND. The following chart summarizes the impedance options available at each input location.

AMP-IN-X-1 = 100 Ω when AMP-IN-X-2 is open.
AMP-IN-X-1 = 50 Ω when AMP-IN-X-2 is shorted to GND.
AMP-IN-X-2 = 200 Ω when AMP-IN-X-1 is open.

Each channel has two analog inputs AMP-IN-A-1 and AMP-IN-A-2 or AMP-IN-B-1 and AMP-IN-B-2. Use AMP-IN-A-1 or

AMP-IN-B-1 when an input of ±0.5 V full scale is desired. Use AMP-IN-A-2 or AMP-IN-B-2 when ±1 V full scale is desired. Each channel has an AMP-OUT that must be tied to either a noninverting or inverting input of a differential amplifier with the remaining input grounded. For example, Side A, AMP-OUT-A (Pin 6) must be tied to A+IN (Pin 5) with A–IN (Pin 4) tied to ground for noninverting operation or AMP-OUT-A (Pin 6) tied to A–IN (Pin 4) with A+IN (Pin 5) tied to ground for inverting operation.

USING THE DIFFERENTIAL INPUT

Each channel of the AD13280 was designed with two optional differential inputs, A+IN, A–IN and B+IN, B–IN. The inputs provide system designers with the ability to bypass the AD8037 amplifier and drive the AD8138 directly. The AD8138 differential ADC driver can be deployed in either a single-ended or differential input configuration. The differential analog inputs have a nominal input impedance of 620 Ω and nominal full-scale input range of 1.2 V p-p. The AD8138 amplifier drives a differential filter and the custom analog-to-digital converter. The differential input configuration provides the lowest even-order harmonics and signal-to-noise (SNR) performance improvement of up to 3 dB (SNR = 73 dBFS). Exceptional care was taken in the layout of the differential input signal paths. The differential input transmission line characteristics are matched and balanced. Equal attention to system level signal paths must be provided in order to realize significant performance improvements.

APPLYING THE AD13280

Encoding the AD13280

The AD13280 encode signal must be a high quality, extremely low phase noise source, to prevent degradation of performance. Maintaining 12-bit accuracy at 80 MSPS places a premium on encode clock phase noise. SNR performance can easily degrade 3 dB to 4 dB with 37 MHz input signals when using a high jitter clock source. See Analog Devices' Application Note AN-501, *Aperture Uncertainty and ADC System Performance,* for complete details. For optimum performance, the AD13280 must be clocked differentially. The encode signal is usually ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 6 shows one preferred method for clocking the AD13280. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD13280 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to the other portions of the AD13280, and limits the noise presented to the ENCODE inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limited resistor (typically 100 Ω) is placed in the series with the primary.

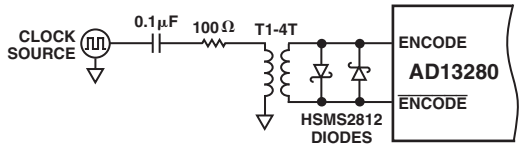


Figure 6. Crystal Clock Oscillator—Differential Encode

If a low jitter ECL/PECL clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown below. A device that offers excellent jitter performance is the MC100LVEL16 (or same family) from Motorola.

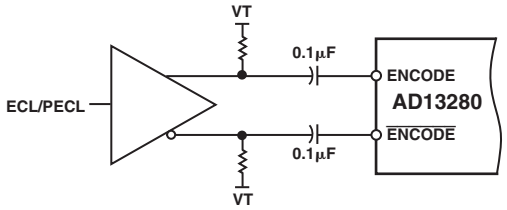


Figure 7. Differential ECL for Encode

Jitter Consideration

The signal-to-noise ratio (SNR) for any ADC can be predicted. When normalized to ADC codes, Equation 1 accurately predicts the *SNR* based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

$$SNR = -20 \times \log\left[\left[\frac{(1+\varepsilon)}{2^N}\right] + (2 \times \pi \times f_{ANALOG} \times t_{J\,rms})^2 + \left(\frac{V_{NOISE\,rms}}{2^N}\right)^2\right]^{1/2} \quad (1)$$

f_{ANALOG} = analog input frequency

$t_{J\,rms}$ = rms jitter of the encode (rms sum of encode source and internal encode circuitry)

ε = average DNL of the ADC (typically 0.50 LSB)

N = number of bits in the ADC

$V_{NOISE\,rms}$ = the analog input of the ADC (typically 5 LSB)

For a 12-bit analog-to-digital converter like the AD13280, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. The chart below shows a family of curves that demonstrates the expected SNR performance of the AD13280 as jitter increases. The chart is derived from Equation 1.

For a complete discussion of aperture jitter, please consult Analog Devices' Application Note AN-501, *Aperture Uncertainty and ADC System Performance.*

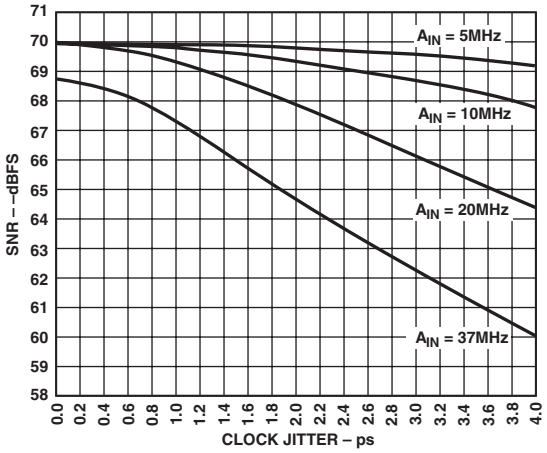


Figure 8. SNR vs. Jitter

Power Supplies

Care should be taken when selecting a power source. Linear supplies are strongly recommended. Switching supplies tend to have radiated components that may be "received" by the AD13280. Each of the power supply pins should be decoupled as closely as possible to the package, using 0.1 µF chip capacitors.

The AD13280 has separate digital and analog power supply pins. The analog supplies are denoted AV_{CC} and the digital supply pins are denoted DV_{CC}. AV_{CC} and DV_{CC} should be separate power supplies because the fast digital output swings can couple switching current back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 V. The AD13280 is specified for DV_{CC} = 3.3 V as this is a common supply for digital ASICs.

Output Loading

Care must be taken when designing the data receivers for the AD13280. The digital outputs drive an internal series resistor (e.g., 100 Ω) followed by a gate like 75LCX574. To minimize capacitive loading, there should be only one gate on each output pin. An example of this is shown in the evaluation board schematic (Figure 9). The digital outputs of the AD13280 have a constant output slew rate of 1 V/ns. A typical CMOS gate combined with a PCB trace will have a load of approximately 10 pF. Therefore, as each bit switches, 10 mA (10 pF × 1 V ÷ 1 ns) of dynamic current per bit will flow in or out of the device. A full-scale transition can cause up to 120 mA (12 bits × 10 mA/bit) of transient current through the output stages. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD13280. It should also be noted that extra capacitive loading will increase output timing and invalidate timing specifications. Digital output timing is guaranteed with 10 pF loads.

EVALUATION BOARD

The AD13280 evaluation board (Figure 9) is designed to provide optimal performance for evaluation of the AD13280 analog-to-digital converter. The board encompasses everything needed to ensure the highest level of performance for evaluating the AD13280. The board requires an analog input signal, encode clock, and power supply inputs. The clock is buffered on-board to provide clocks for the latches. The digital outputs and out clocks are available at the standard 40-pin connectors J1 and J2.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the associated components and the analog section of the AD13280. The digital outputs of the AD13280 are powered via banana jacks with 3.3 V. Contact the factory if additional layout or applications assistance is required.

LAYOUT INFORMATION

The schematics of the evaluation board (Figures 10a–10c) represent a typical implementation of the AD13280. The pinout of the AD13280 is very straightforward and facilitates ease of use and the implementation of high frequency/high resolution design practices. It is recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. All capacitors can be standard high quality ceramic chip capacitors.

Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate. Internal circuitry buffers the outputs of the ADC through a resistor network to eliminate the need to externally isolate the device from the receiving gate.

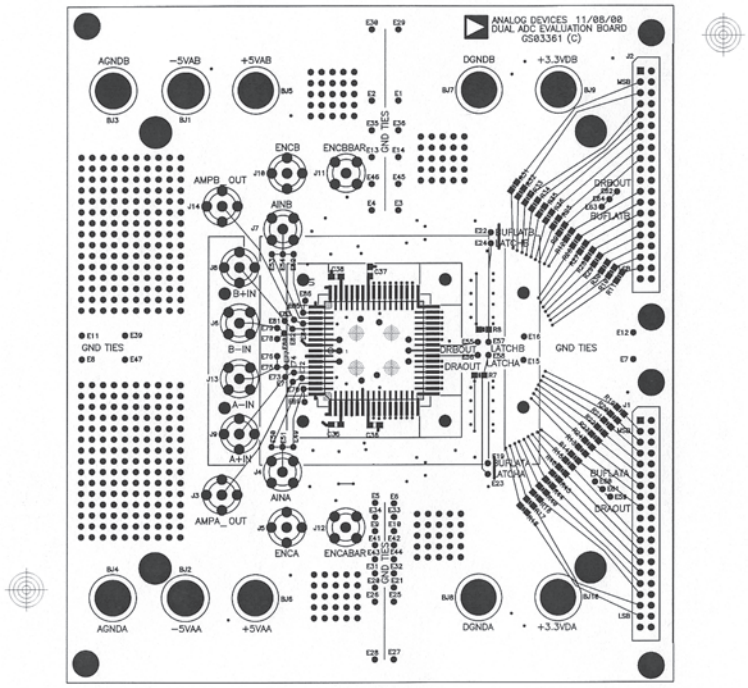


Figure 9. Evaluation Board Mechanical Layout

Bill of Materials List for Evaluation Board

Qty.	Component Name	Ref/Des	Value	Description	Manufacturing Part Number
2	74LCX16373MTD	U7, U8		Latch	74LCX16373MTD (Fairchild)
1	AD13280AZ	U1		AD13280	AD13280AZ
2	ADP3330	U5, U6		Regulator	ADP3330ART-3.3RL7
10	BJACK	BJ1–BJ10		Banana Jacks	108-0740-001 (Johnson Components)
2	BRES0805	R41, R53	25 Ω	0805 SM Resistor	ERJ-6GEYJ 240V
4	BRES0805	R38, R39, R55, R56	33 kΩ	0805 SM Resistor	ERJ-6GEYJ 333V
28	CAP2	C1, C2, C5–C10, C12, C16–C18, C20–C26, C28, C30–C38	0.1 µF	0805 SM Capacitor	GRM 40X7R104K025BL
2	CAP2	C13, C27	0.47 µF	0805 SM Capacitor	VJ1206U474MFXMB
2	H40DM	J1, J2		2 × 20 40 Pin Male Connector	TSW-120-08-G-D
6	IND2	L1–L6	47 Ω	SM Inductor	2743019447
4	MC10EL16	U2, U4, U9, U11		Clock Drivers	MC1016EP16D
2	MC100ELT23	U4, U10		ECL/TTL Clock Drivers	SY100ELT23L
8	POLCAP2	C3, C4, C11, C14, C15, C19, C29, C30	10 µF	Tantalum Polar Caps	T491C106M016A57280
4	RES2	R47–R50	0 Ω	0805 SM Resistor	ERJ-6GEY OR 00V
6	RES2	R1, R2, R5, R7, R8, R54	50 Ω	0805 SM Resistor	ERJ-6GEYJ 510V
36	RES2	R3, R4, R6, R9, R12–R15, R19–R28, R31–R36, R37, R42, R43, R44–R46 R51, R52	100 Ω	0805 SM Resistor	ERJ-6GEYJ 101V
12	SMA	J3–J14		SMA Connectors	142-0701-201
4	Standoff			Standoff	313-2477-016 (Johnson Components)
4	Screws			Screws (Standoff)	MPMS 004 0005 PH (Building Fasteners)
1	PCB			AD13280 Eval Board (Rev. B)	GS03361

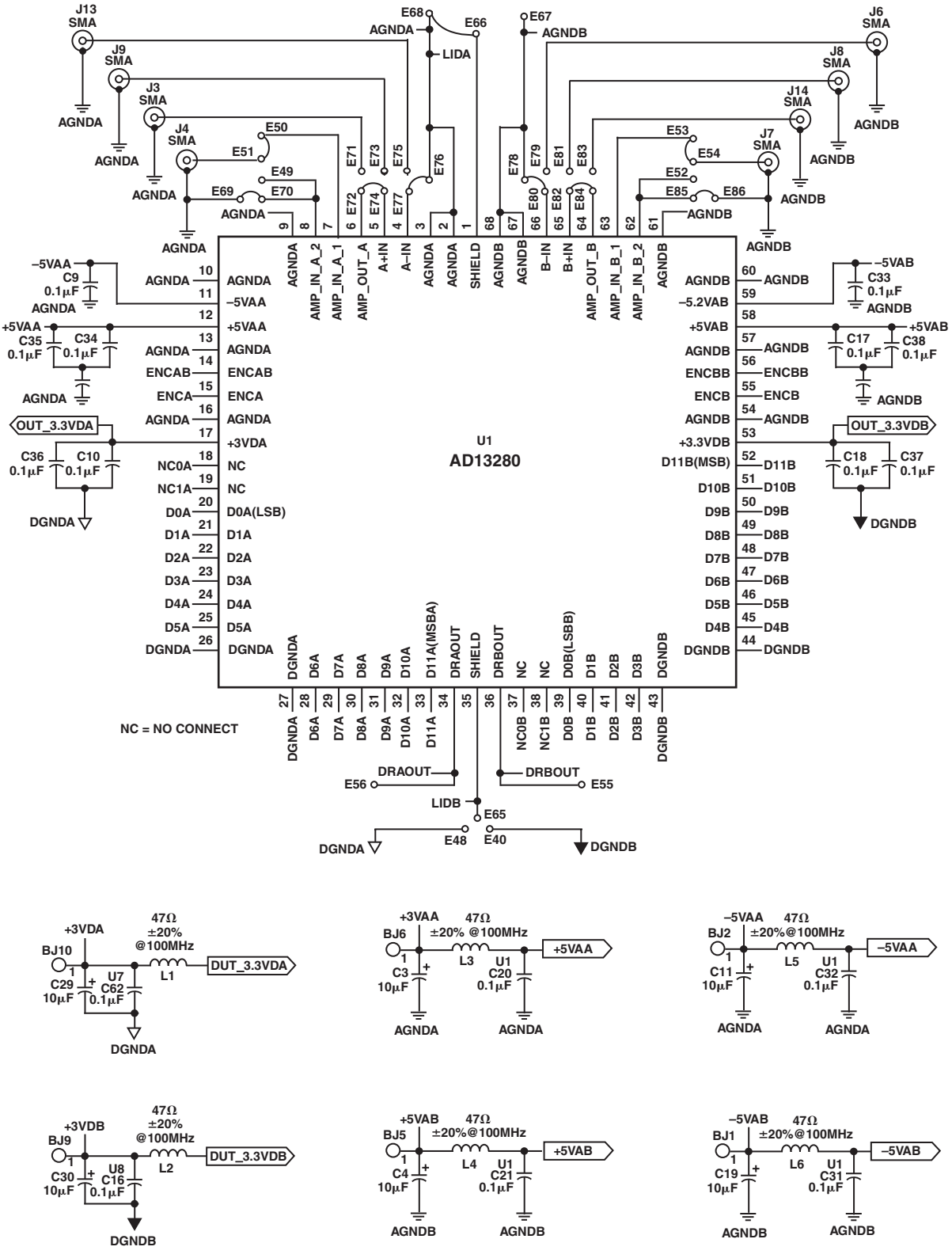


Figure 10a. Evaluation Board

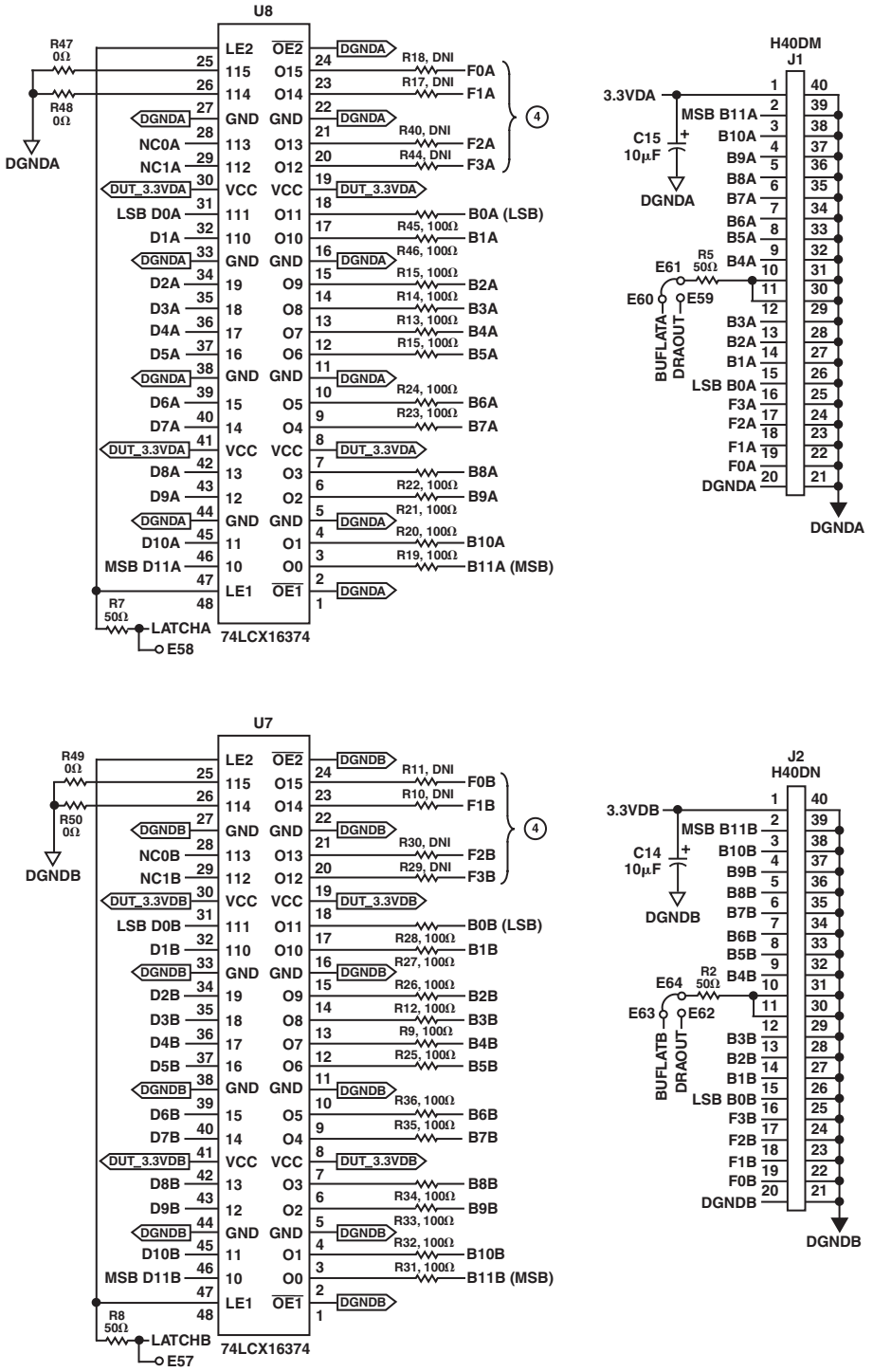


Figure 10b. Evaluation Board

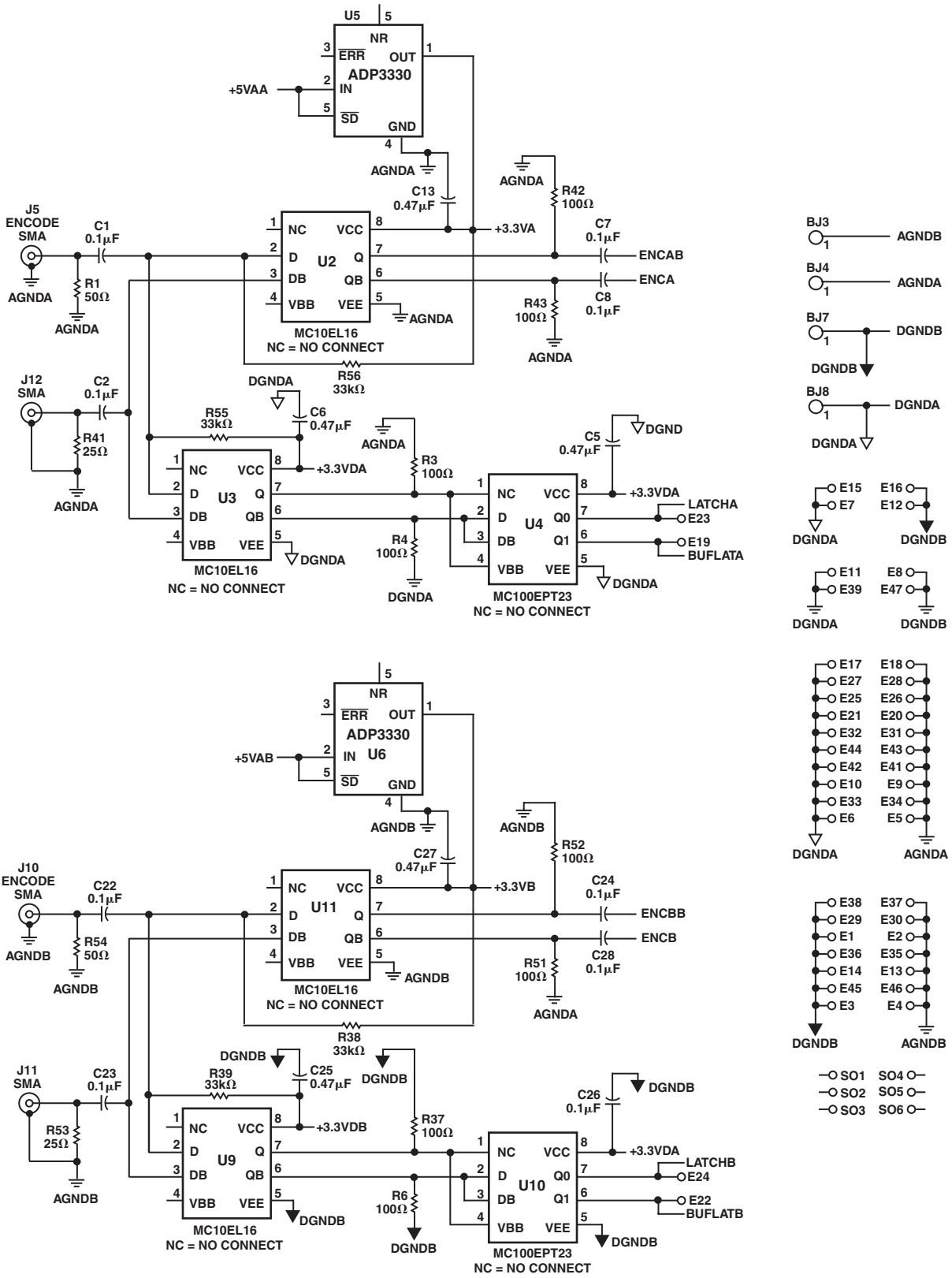


Figure 10c. Evaluation Board

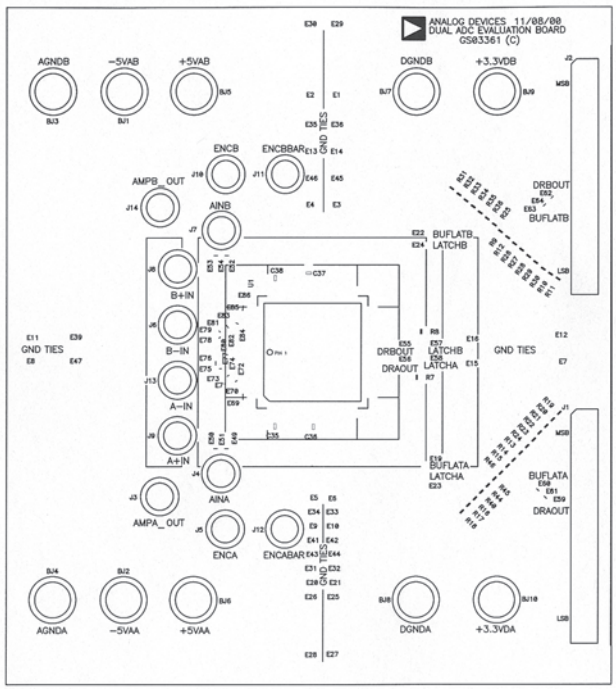


Figure 11a. Top Silk

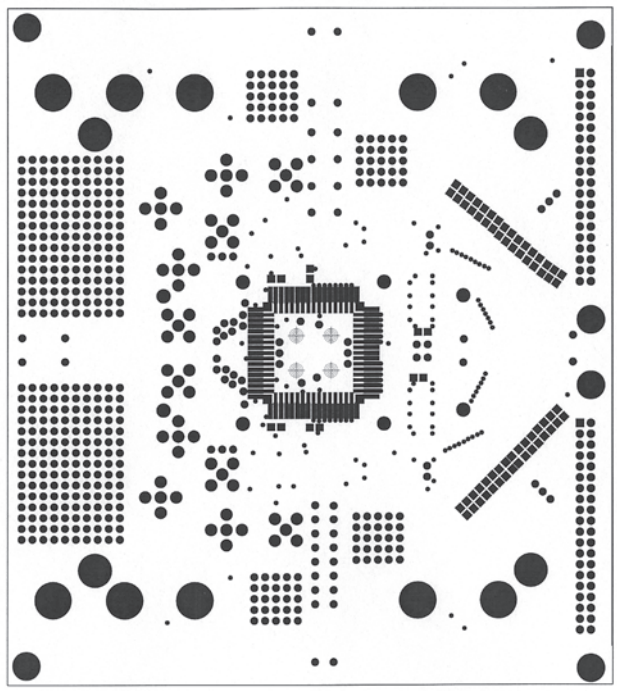


Figure 11b. Top Layer

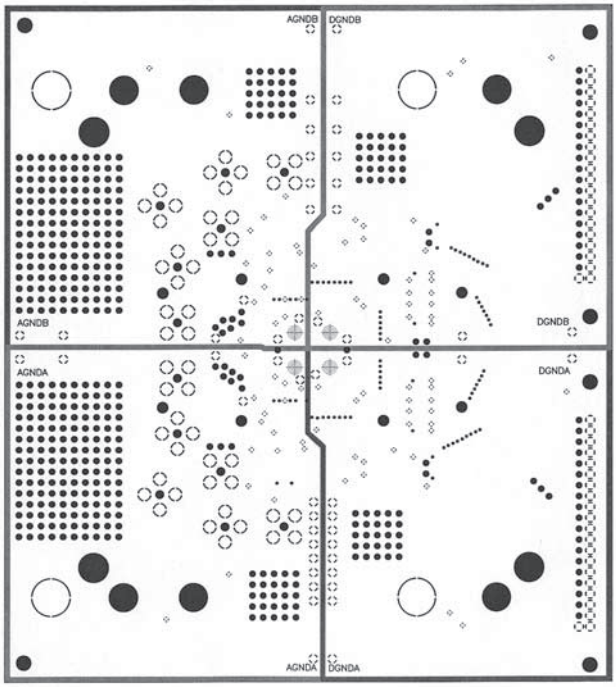


Figure 11c. GND1

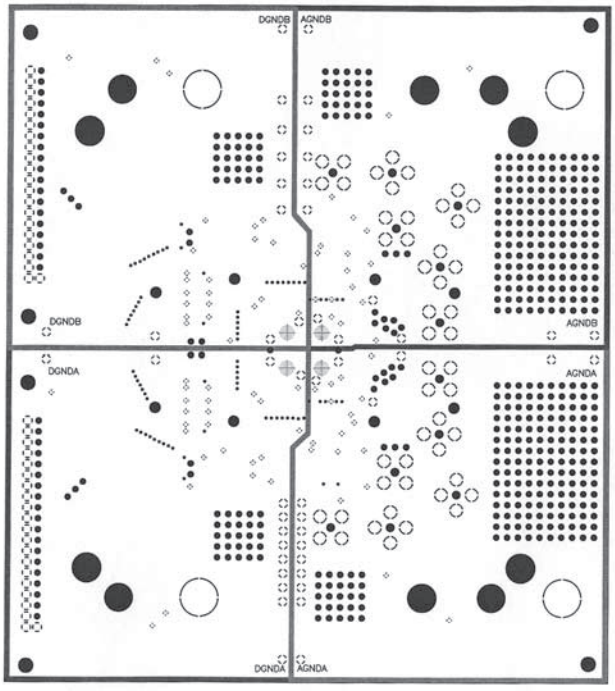


Figure 11d. GND2

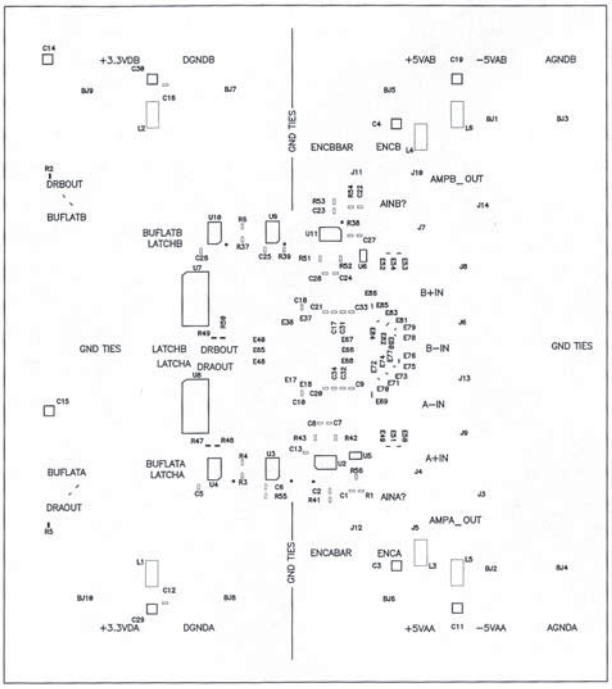


Figure 11e. Bottom Silk

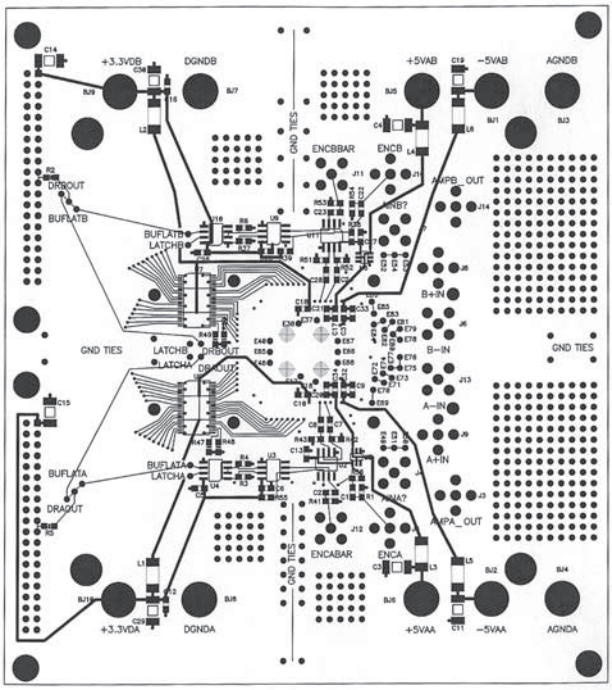
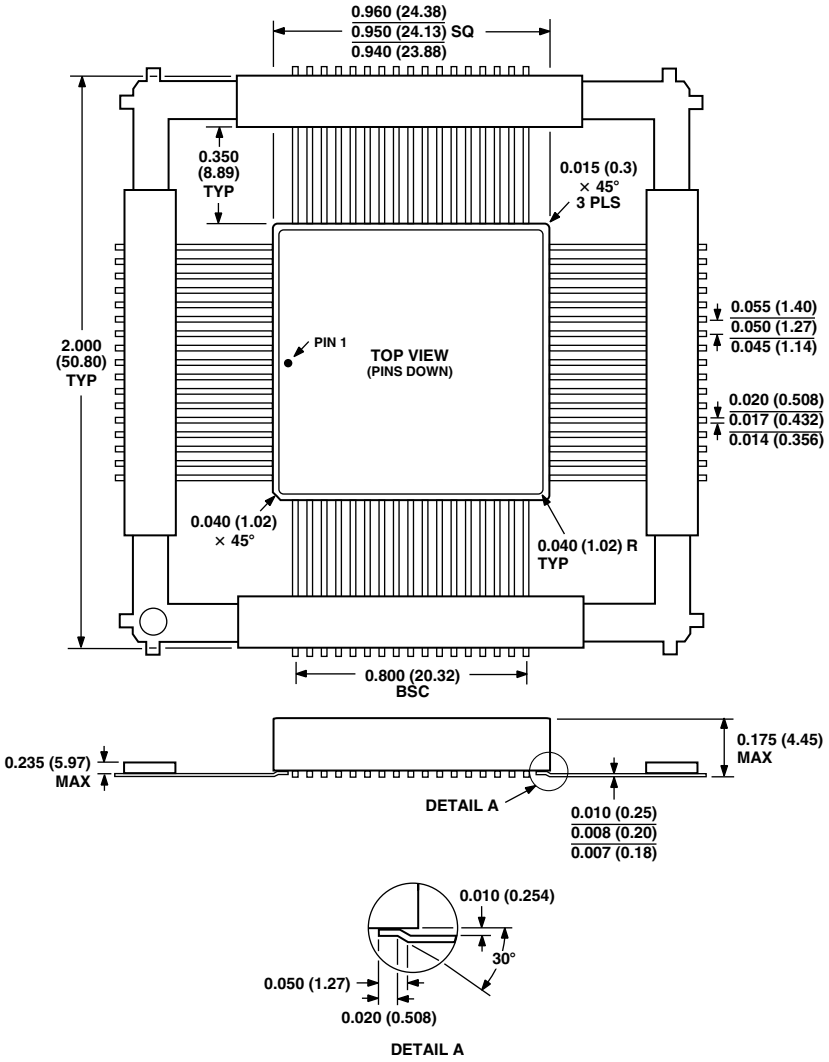


Figure 11f. Bottom Layer

OUTLINE DIMENSIONS

68-Lead Ceramic Leaded Chip Carrier with Nonconductive Tie-Bar (ES-68C)

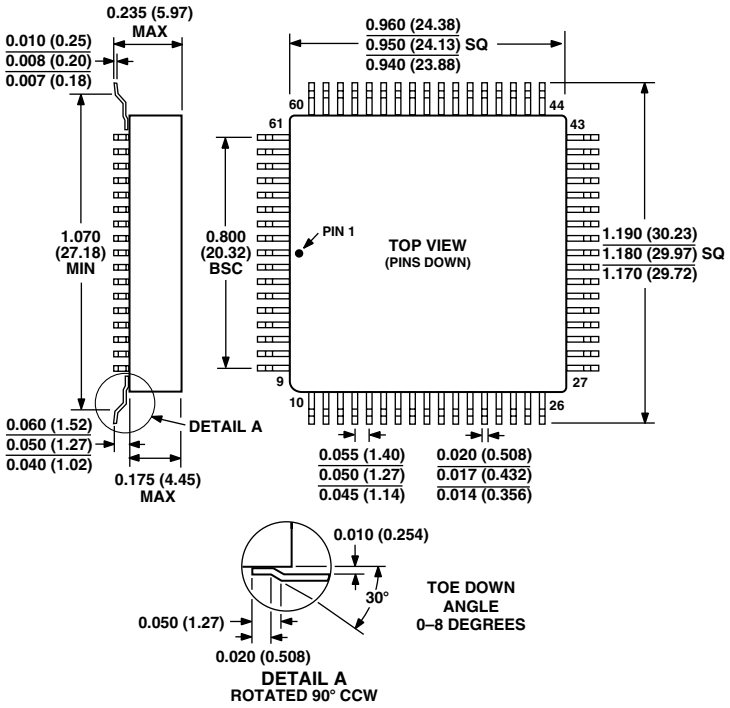
Dimensions shown in inches and (millimeters)



OUTLINE DIMENSIONS

68-Lead Ceramic Leaded Chip Carrier [CLCC]
(ES-68C)

Dimensions shown in inches and (millimeters)



Revision History

Location	Page
8/02–Data Sheet changed from REV. 0 to REV. A.	
Edits to SPECIFICATIONS	2
Packages updated	19